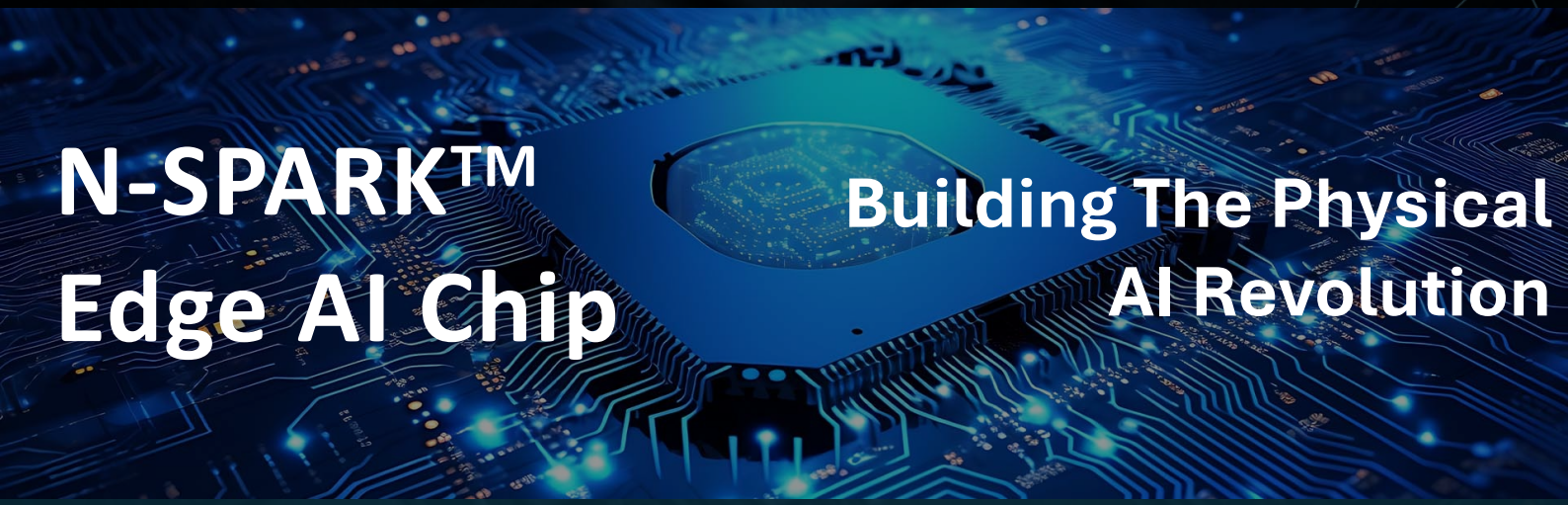


N-SPARK™ Edge AI Chip

Building The Physical AI Revolution

Next generation of smart systems, cameras, robots, drones, requiring fully local LLM with minimal latency and power

HARDWARE

- **Nellow SPARK™** edge AI CV/audio perception + SLM/VLM architecture for immediate risk identification
- AI accelerator for vision, audio, language, multimodal fusion
- Ultra-dense memory enabling ultra-low power in-memory computing
- CMOS-compatible for scalable manufacturing and cost effective
- Hardware-enforced security (secure enclave)

SOFTWARE

- **Nellow ORBIT™ complete SDK for** optimization, compilation & deployment (runtime)
- SystemC Virtual Platform for customer model performances exploration
- Supports quantized SLM/VLM (<4B),
- OS support: Yocto-based BSP + RT AI, FreeRTOS
- **Multimodal framework** vision + audio + sensors + language

Smart Vision / Perception

- Real-time detection & captioning, no cloud cost
- High-precision defect detection, offline mode
- Privacy-preserving cashier less systems

Autonomous Robotics

- Collaborative robot safety, predictive maintenance
- Autonomous navigation in warehouses
- Elderly assist robots with speech + vision

Drones / UAV

- Safer autonomous missions
- No RF link required for intelligence
- Longer flight time

Industrial Edge

- Perception + SLM/VLM reasoning locally
- Human-machine voice interfaces
- Factory safety monitoring

GLOBAL ARCHITECTURE

- ✓ Sustainable Edge AI
- ✓ BoM reduction
- ✓ Time-To-Market
- ✓ Sovereign Data Privacy

Perception & reasoning

100mW power consumption

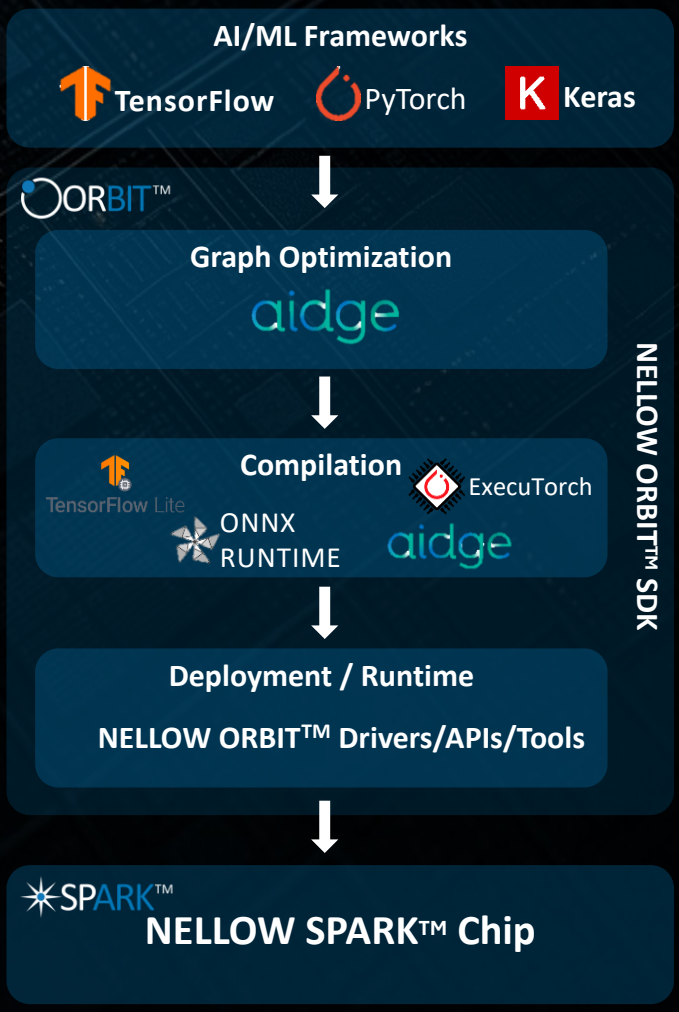
Real-time applications

Security

KEY CHARACTERISTICS

Architecture	N-FLUX™ Edge AI architecture for real-time reasoning applications. Data compression & cache management. Auto-adaptive coarse & fine grain power management
AI/ML	+30 TOPS performance, 25+ TOPS/W, Time-to-First Token 100ms, 30 tk/s latency, INT4 → BP16 operations
Power Consumption	<100mW average power consumption for CV + SLM/VLM execution
On-Chip Memory	High amount of NVM to store weights + SRAM + context memories
External Interfaces	**Memory:** HSPI with inline AES decryption, XIP. Optional LPDDR5
	Cameras: 2 x MIPI CSI-2 (2-lanes), 1 x DSI
	Analog Interfaces: ADCs: 12-bit & 24-bit + DACs: 12-bit
	Serial Interfaces: 32xGPIOs, xSPI M/S, I3C/I2C, PWM, SWD & JTAG, UART
	Internal Peripherals: LP timers, ADV timers, WDT, HW SEM, RTC
Security	Secure boot with an immutable Root-of-Trust, HW cryptographic services, RDP, secured OTA firmware updates

SOFTWARE DESIGN KIT



ROADMAP

NELLOW
17 Avenue des Martyrs
38000 Grenoble, FRANCE
https://nellow.eu
contact@nellow.eu

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